**CT3 -QUESTIONS**

**PART A**

1. Executing two or more operations at the same time is known as --------

a) Distributed processing

b) Pipe processing

c) Parallel processing

d) multi processing

2. ---------displays the patterns of simultaneously executable operations.

a) flow graph

b)program flow graph

c) program flow chart

d) flow chart

3. consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many load instructions required for this?

a)8

b)4

c)2

d)1

4. Hardware Parallelism can be achieved through

a) Parallel processor

b) multi processor

c)k-issue processor

d) pipeline processor

5. TWO-issue processors are capable of doing-------------

a) one memory access(Load/Store) and two arithmetic operation

b) two memory access(Load/Store) and one arithmetic operation

c) two memory access(Load/Store) and two arithmetic operation

d)one memory access and one arithmetic operation

6. Executing several instructions per clock cycle is \_\_\_\_\_\_\_\_\_\_\_\_ while overlapping of multiple instructions is \_\_\_\_\_\_\_\_\_\_\_.

a) Parallel processor, pipeline processor

b) multi processor, pipeline processor

c)pipeline processor, k-issue processor

d) pipeline processor, Parallel processor

7. Which of the following is true?

a)pipeline processors have lower performance than Parallel processor

b) Parallel processors have lower performance than pipeline processor

c)Parallel processors and pipeline processor have lower performance

d) Parallel processors and pipeline processor have more performance pipeline processor

8. ---------Pushes only one instruction to next stage / clock cycle.

a) Parallel processors

b) pipeline processors

c) multi processors

d)k-issue processors

9) What type of hazards are identified in the following instructions ?

x= a+b ; y=c-d; z=x \* y

a) Data hazards

b)Control Hazards.

c)Instruction Hazards.

d) pipeline Hazards.

10) ----------plays an important part in evaluating the performance of a data parallel programming model.

a) Locality of Reference

b) memory Reference

c) data reference

d) instruction reference

11) Flynn's taxonomy are based on----------------------

a) main memory size

b) the number of concurrent instruction and data

c) cache memory size

d) both on (a) and (c)

12) \_\_\_\_\_\_\_\_\_\_\_\_\_does not have parallel processing capabilities

a)SIMD

b)SISD

c)MISD

d)MIMD

13) Which of the following holds true with respect to Cache memory

a) It has greater capacity than RAM

b) It is faster to access than CPU Registers

c) It is permanent storage

d) It is faster to access than RAM

14)Most commonly used cache coherence protocol is

a)MOESI protocol

b)MESI protocol

c)MSI protocol

d)MOSI protocol

15) A thread comprises of

a) Thread id

b) program counter

c) stack, and a set of registers

d) All of the above

16) In Hardware Multithreading execution of multiple thread is supported by

a) CPU

b) OS

c) Cache

d) None of the above

17) Cache Coherence Problem arises with respect to \_\_\_\_\_\_\_\_\_\_\_\_

a)Sharing of writable data.

b) updating data in cache.

c)Inconsistency due to I/O

d)All of these

18) Switches between threads on each instruction is happened in

a) multi threading

b) coarse grained multi threading

c) Fine grained multi threading

d) Fine and coarse grained multi threading

19) Which of the following holds true in the context of multicore processors?

a) They are MIMD

b) all cores share the same memory

c) They are shared memory multiprocessor

d) all the above

20) In NUMA, the Shared memory that is physically distributed among all the processors are called ------

a) local memories.

b) remote memories.

c) cache memories.

d) None of the above

**PART B**

1.Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many machine cycles required for the parallel execution? (consider the Software Parallelism)

a)12

b)4

c)6

d)3

2. Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 How many machine cycles required for the parallel execution? (consider the H/W Parallelism with 2-issue processor)

a)12

b)4

c)7

d)3

3. How much units of time required to complete the following operationswhen they are executed in Instruction level parallelism manner?

x= a+b ; y=c-d; z=x \* y

a)2

b)4

c)1

d)3

4) Which of the following holds true with respect to UMA and NUMA?

a) No memory controller in UMA and NUMA

b) single memory controller in NUMA and multiple memory controller in UMA

c) Multiple memory controller in UMA and multiple memory controller in NUMA

d) single memory controller in UMA and multiple memory controller in NUMA

5) Processors have their own local memory and operates independently are called

a)Distributed memory computers

b)ccNUMA systems

c)nccNUMA systems

d)Symmetric multiprocessors

6) which of the following is correct w.r.to these instructions

(i) x= a+b ; (ii) y=c-d; (iii) z=x \* y

a) (i) and (ii) can be computed simultaneously.

b) (i) and (ii) cannot be computed simultaneously.

c) (iii) cannot be calculated until (i) and (ii) are calculated

d) both (a) and (c) are correct

7) which of the following ensures data consistency between the cache memory and the shared memory

a)bus protocol

b) SI protocol

**c) Snoopy bus protocols**

**d) seven layer** protocol

8) The policies used for maintaining cache consistency by **Snoopy bus protocols are** .

a) Write-invalidate policy

b) Write-read policy

c) Write-update policy

d) both (a) and (c)

9) Invalidate/  **dirty** bit in Write-invalidate policy represent

a) they can be used in near future

b)they should not be used at all

c) they can be modified

d) they cannot be modified

10) Under which policy, the processor that is writing the data can broadcasts the new data over the bus without issuing the invalidation signal

a) Write-invalidate policy

b) Write-read policy

c) Write-update policy

d) both (a) and (c)

11) ----------------includes many processing units under the supervision of a common control unit.

a)SIMD

b)SISD

c)MISD

d)MIMD

12)---------- is always performed in local cache memory without causing a transition of state

a)Read Miss

b)Write Hit

c)Read Hit

d) Write Miss

13 ) locality of reference in the memory systems are

a) Temporal

b)spatial

c)sequential

d) All of the above

14)MROM (mask ROM) and **PROM (programmable ROM) stands**

a) Mask ROM and Parallel ROM

b) Memory ROM and Programmable ROM

c) Mask ROM and Programmable ROM

d) None of the above

15) Cache between main memory and processor and caches on the processor chip and are

a) L2 and L1

b) L1 and L2

c) L1 and L3

d) L2 and L3

16) Page fault occurs when

a)a requested page is in memory

b)a requested page is not in memory

c)a page is corrupted

d)None of the above

17) In which mapping, the data can be mapped anywhere in the cache memory?

a)Associative

b)Direct

c)Set Associative

d)Indirect

18) Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?

a)Write through

b)Write back

c)Both write through and write back

d)Cycle Stealing

19) ---------- is the memory access where all the processors share the physical memory in a centralized manner with equal access time to all the memory words.

a) NUMA.

b) NC-NUMA

c) UMA

d) CC-NUMA

20) Many software packages that run on windows are multithreaded. State true or false.

a) True

b) False

21) Interleaved execution of multiple threads in a round-robin fashion occurs in

a) coarse grained multi threading

b) Fine grained multi threading

c) Fine and coarse grained multi threading

d) multi threading

22)----------has separate data cache and a separate instruction cache.

a)direct-mapped cache

b)Dual cache

c)Split cache

d)fully associative cache

23)MESI protocol enforcing data integrity among caches sharing data through

a) Write back scheme

b) dirty data

c) clean data

d) both (a) and (b)

24) In which mapping, the cache memory has to be very frequently replaced even when other blocks in the cache memory were present as empty?

a)Indirect mapping

b) Fully Associative mapping

c) Set Associative mapping

d)Direct mapping

25) In Set Associative mapping, memory blocks are mapped into following cache set

a) Total no.of sets %memory block number

b) memory block number % Total no.of sets

c) Total no.of sets %cache line number

d) cache line number % Total no.of sets

**Part C**

1)Assuming a 15-bit address space with 8 logical pages. How large are the pages?

a) 2 power 10

b)2 power 11

c) 2 power 12

d) 2 power 15

2) Find the hit ratio and miss ratio of the cache when there was 9 hits and 5 misses.

a) 14/9 and 14/5

b)14/5 and 14/9

c) 9/14 and 5/14

d) 5/14 and 9/14

3) Consider the instructions

A=X1\*X2+X3\*X4

B=X1\*X2-X3\*X4 What is the H/w parallelism average?

a)8/6

b)12/4

c)7/8

d)8/7

4) How many tag bits are needed to map 16KB main memory/ to 1KB cache? Consider the word offset to be 4 bits.

a) 4

b) 6

c) 2

d) 12

5) Consider the following reference string. Calculate the number of page faults when the page frame size is 4 using LRU policy.

1,2,3,4,2,1,5,6,2,1,2,3,7,6

a) 4

b) 5

c) 14

d) 9